

## 4P0305-VB TO263 Datasheet

### P-Channel 30-V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>d</sup>	$Q_g$ (Typ.)
- 30	0.005 at $V_{GS} = -10$ V	- 100	60nC
	0.006 at $V_{GS} = -4.5$ V	- 85	

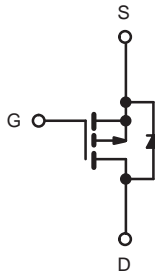
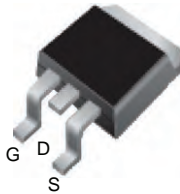
#### FEATURES

- Halogen-free
- Trench Power MOSFET
- 100 %  $R_g$  Tested
- 100 % UIS Tested


**RoHS**  
 COMPLIANT

#### APPLICATIONS

- Load Switch
- Notebook Adaptor Switch

D<sup>2</sup>PAK (TO-263)

P-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	- 100	A
	$T_C = 70$ °C	- 85	
	$T_A = 25$ °C	-68 <sup>a, b</sup>	
	$T_A = 70$ °C	-56 <sup>a, b</sup>	
Pulsed Drain Current	$I_{DM}$	- 260	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 4.8	
	$T_A = 25$ °C	- 2.5 <sup>a, b</sup>	
Avalanche Current	$I_{AS}$	- 80	
Single-Pulse Avalanche Energy	$E_{AS}$	280	mJ
Maximum Power Dissipation	$T_C = 25$ °C	254	W
	$T_C = 70$ °C	225	
	$T_A = 25$ °C	4.0 <sup>a, b</sup>	
	$T_A = 70$ °C	2.8 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, c</sup>	$R_{thJA}$	38	46	°C/W
Maximum Junction-to-Foot	$R_{thJF}$	20	25	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b.  $t = 10$  s.

c. Maximum under Steady State conditions is 85 °C/W.

d. Based on  $T_C = 25$  °C.

SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 30			V		
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 34		mV/ °C		
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			-5.3				
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1.0		- 2.5	V		
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 25 V			± 100	nA		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1	μA		
		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5			
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ - 10 V, V <sub>GS</sub> = - 10 V	- 30			A		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A		0.005		Ω		
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 8 A		0.006				
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 10 A		28		S		
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4850		pF		
Output Capacitance	C <sub>oss</sub>			1560				
Reverse Transfer Capacitance	C <sub>rss</sub>			640				
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A		115		nC		
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 10 A		56				
Gate-Drain Charge	Q <sub>gd</sub>			8				
Gate Resistance	R <sub>g</sub>			22				
Turn-On Delay Time	t <sub>d(on)</sub>	f = 1 MHz	0.5	2.2	4.4	Ω		
Rise Time	t <sub>r</sub>		V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≡ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		13		25	ns
Turn-Off DelayTime	t <sub>d(off)</sub>				12		24	
Fall Time	t <sub>f</sub>				40		70	
Turn-On Delay Time	t <sub>d(on)</sub>			9	18			
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≡ - 10 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω			48	80		
Turn-Off DelayTime	t <sub>d(off)</sub>				92	160		
Fall Time	t <sub>f</sub>				34	60		
					19	35		
Drain-Source Body Diode Characteristics								
Continous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 4.6	A		
Pulse Diode Forward Current	I <sub>SM</sub>				- 65			
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 3 A, V <sub>GS</sub> = 0 V		- 0.75	- 1.2	V		
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		27	45	ns		
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			16	27	nC		
Reverse Recovery Fall Time	t <sub>a</sub>			12		ns		
Reverse Recovery Rise Time	t <sub>b</sub>			15				

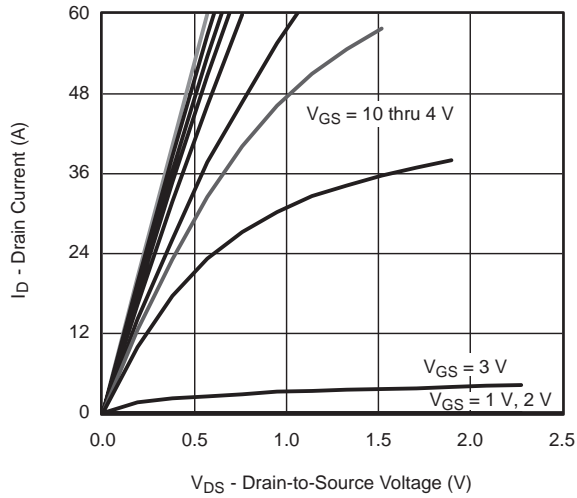
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

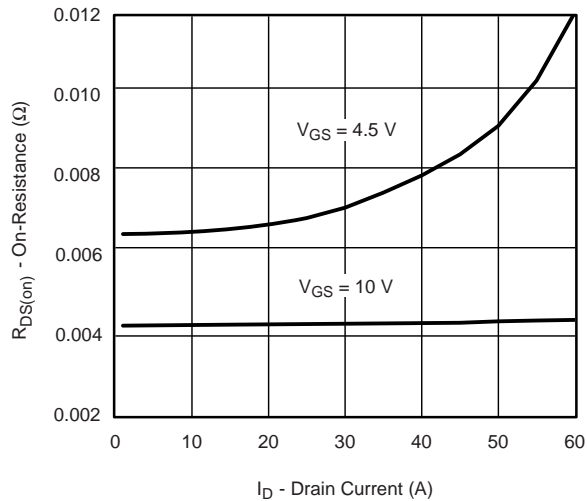
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



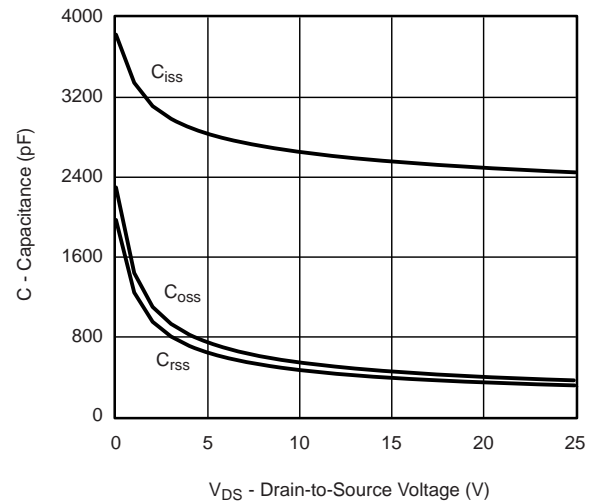
**Output Characteristics**



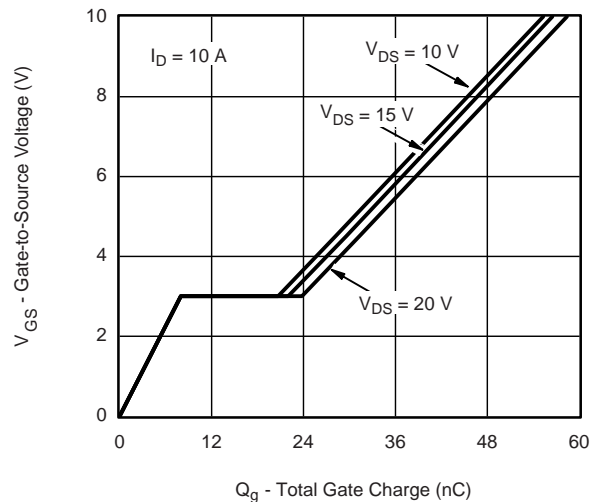
**Transfer Characteristics**



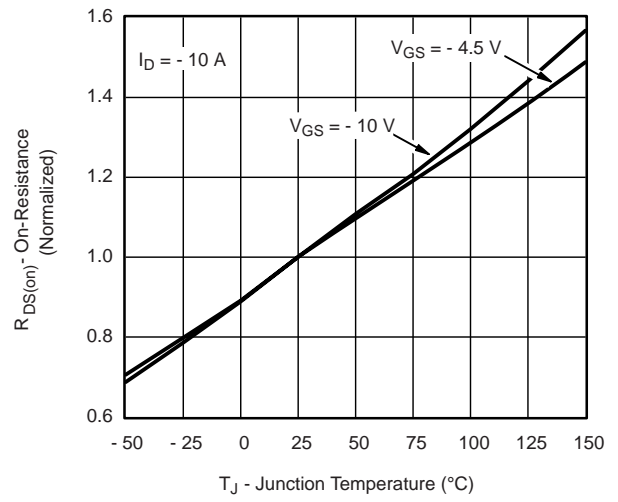
**On-Resistance vs. Drain Current**



**Capacitance**

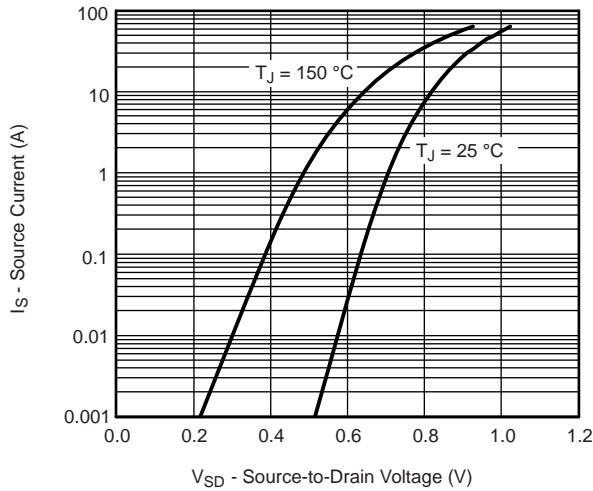


**Gate Charge**

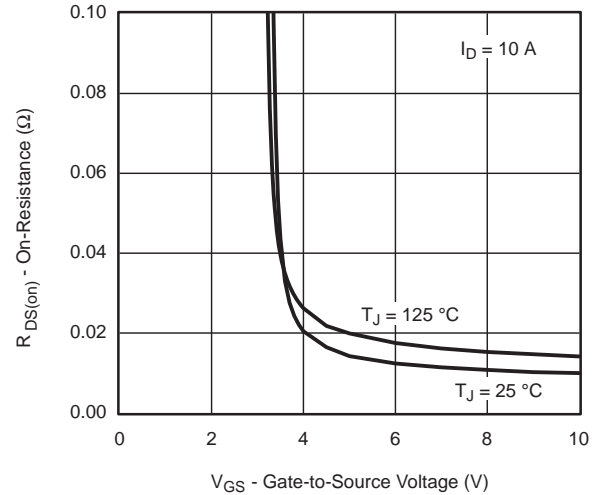


**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



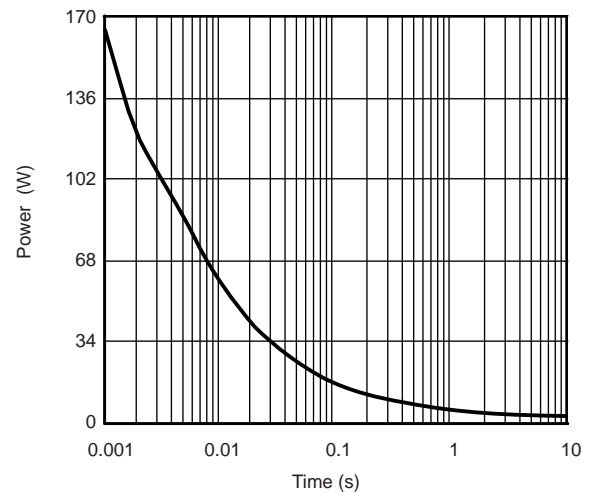
Source-Drain Diode Forward Voltage



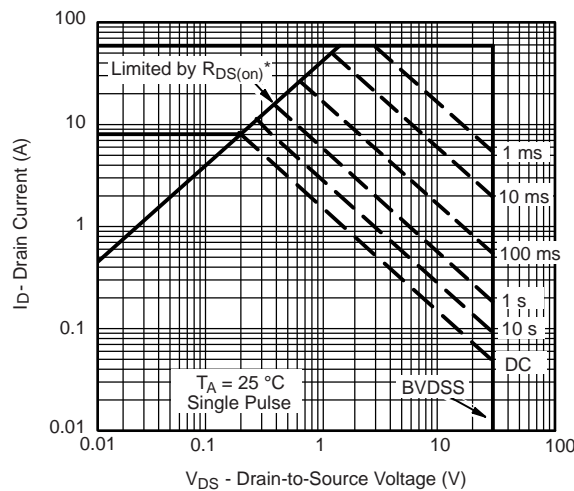
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

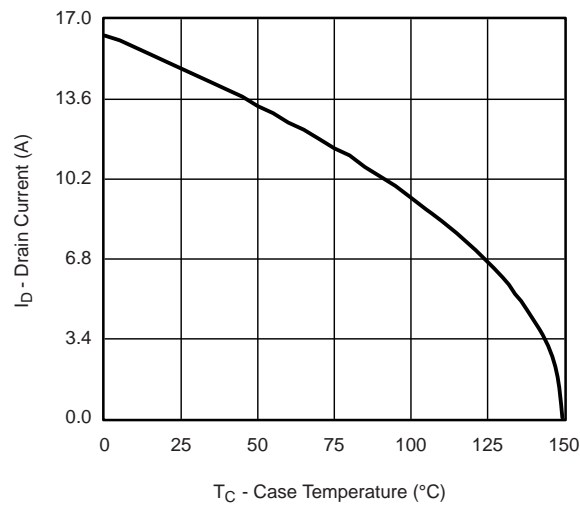
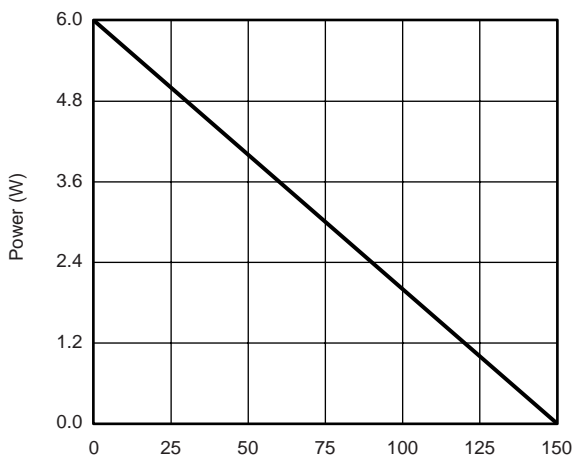
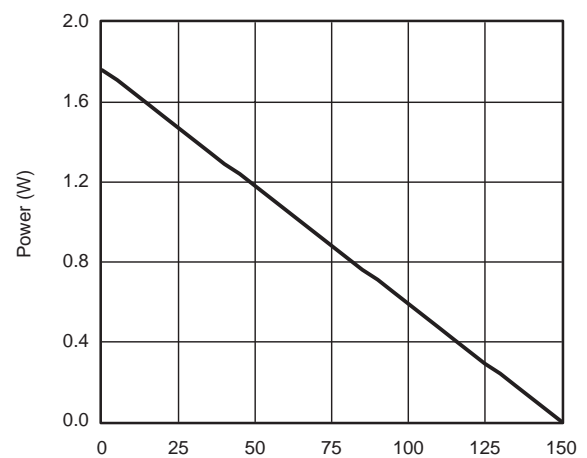


Single Pulse Power, Junction-to-Ambient



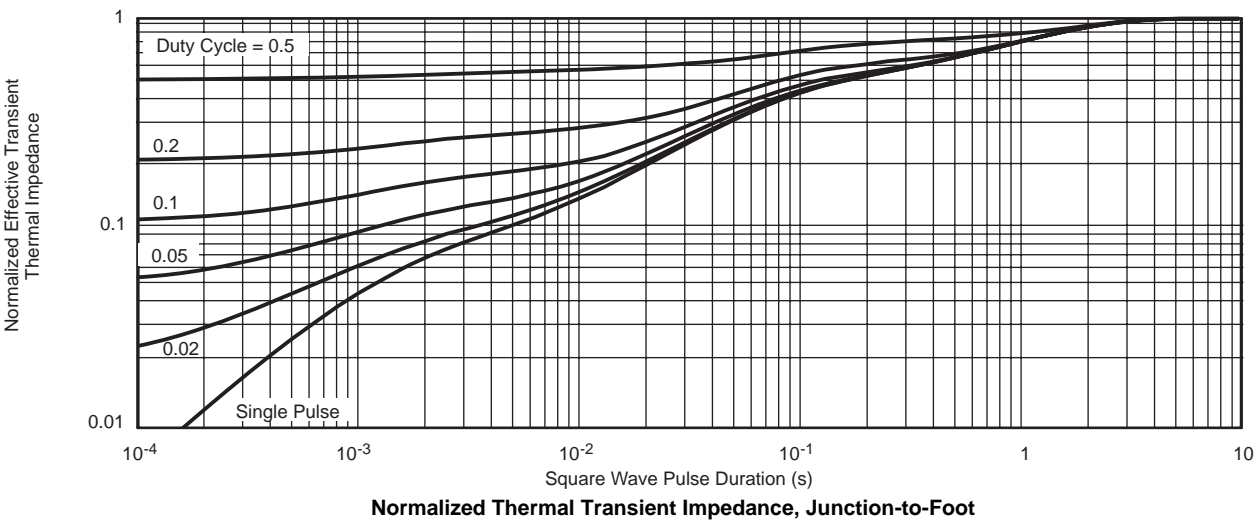
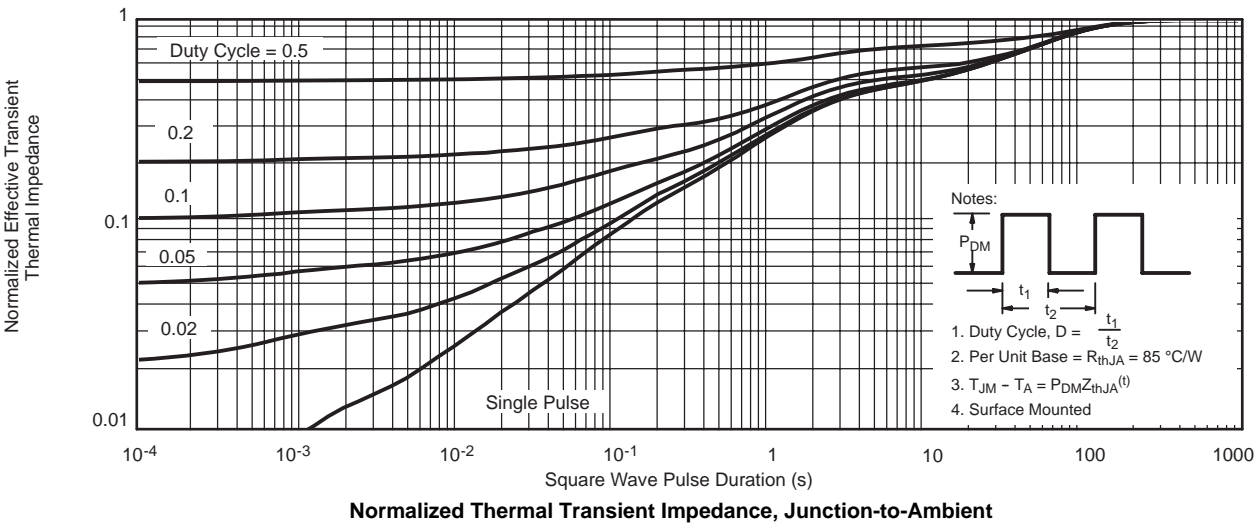
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area

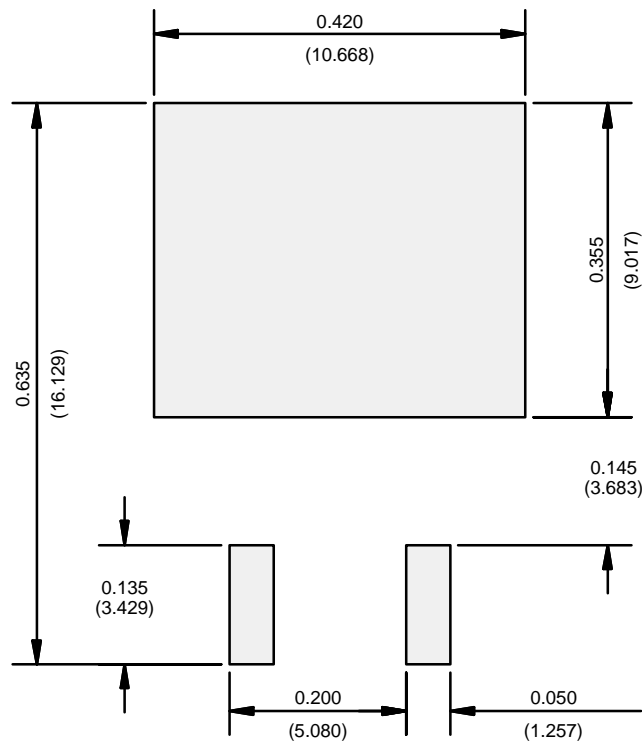
**MOSFET TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Current Derating\***

**Power, Junction-to-Foot**

**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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